536,483

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 June 2004 (10.06.2004)

PCT

(10) International Publication Number
WO 2004/049406 A1

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number:
PCT/US2002/037931

(22) International Filing Date:
25 November 2002 (25.11.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DORIS, Bruce, B.** [US/US]; 350 Lake Shore Drive, Brewster, NY 10509 (US). **CHIDAMBARRAO, Dureseti** [US/US]; 29 Old Mill Road, Weston, CT 06883 (US). **IEONG, Meikei** [PT/US]; 31 Summerlin Court, Wappingers Falls, NY 12590 (US). **MANDELMAN, Jack, A.** [US/US]; 11 Claremont Drive, Flat Rock, NC 28731 (US).

(74) Agent: **ABATE, Joseph, P.**; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

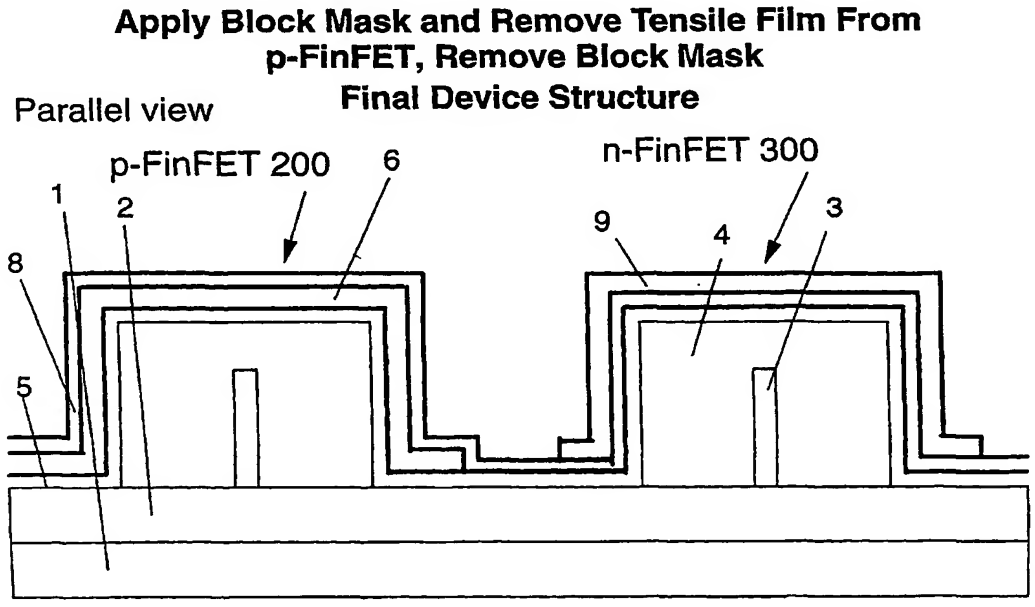
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

[Continued on next page]

(54) Title: STRAINED FINFET CMOS DEVICE STRUCTURES



(57) Abstract: A semiconductor device structure, includes a PMOS device (200) and an NMOS device (300) disposed on a substrate (1, 2) the PMOS device including a compressive layer (6) stressing an active region of the PMOS device, the NMOS device including a tensile layer (9) stressing an active region of the NMOS device, wherein the compressive layer includes a first dielectric material, the tensile layer includes a second dielectric material, and the PMOS and NMOS devices are FinFET devices (200, 300).

WO 2004/049406 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Strained FinFET CMOS Device Structures

Technical Field

The present invention relates to double gate semiconductor device structures and, more particularly, to FinFET devices.

Background Art

Double gate semiconductor device structures are promising candidates for future generation microelectronics devices, because of the ability to obtain near ideal sub-threshold slope, absence of body-effect, immunity to short-channel effect, and very high current driveability. One double gate device structure of technological relevance is the FinFET. The FinFET is particularly attractive because of the relative simplicity of manufacture compared to other double gate devices. The channel for the FinFET is a thin rectangular island of Si, commonly referred to as the Fin. The gate wraps around the Fin so that the channel is gated on both sides of the vertical portions of the Fin structure, providing gate control which is superior to planar single gate MOSFETs.

FinFETs are well known. See, for example, U.S. Patent No. 6,413,802, entitled "FinFET Transistor Structures Having a Double Gate Channel Extending Vertically from a Substrate and Methods of Manufacture" by Hu et al., filed October 23, 2000, issued July 2, 2002, which is hereby incorporated in its entirety by reference. FinFETs having enhanced mobility are also known. See, for example, U.S. Patent Application No.. 2002/0063292 A1, entitled "CMOS Fabrication Process Utilizing Special Transistor Orientation" by Armstrong et al., filed November 29, 2000, published May 30, 2002, which is hereby incorporated in its entirety by reference. This prior art method is directed at improving nFET mobility and, therefor, only limited improvement in CMOS circuits can be attained. Thus, a need exists for a

method to improve mobility for p-FinFETs and n-FinFETs which are situated on the same wafer.

However, the present inventors believe that improvements in utilizing stressing layers to enhance mobility are achievable.

Disclosure of Invention

According to the present invention, a semiconductor device structure includes a PMOS device and an NMOS device disposed on a substrate, the PMOS device including a compressive layer stressing an active region of the PMOS device, the NMOS device including a tensile layer stressing an active region of the NMOS device, wherein the compressive layer includes a first dielectric material, the tensile layer includes a second dielectric material, and the PMOS and NMOS devices are FinFET devices.

This invention is directed to a novel strained FinFET device structures for enhanced mobility. The integration scheme incorporates a new process flow that induces compressive stress in the longitudinal direction for the p-FinFET while also inducing tensile stress in the longitudinal direction for the n-FinFET. These stresses significantly enhance mobility and, thus, enhance device performance. In the invention described herein, the longitudinal stress induced in the channel is enhanced considerably from what can be obtained in standard planar MOSFETs, because the stressing film is applied from two sides of a thin FinFET, instead of on the surface of an SOI layer or bulk substrate.

It is a principal object of the present invention to enhance mobility in double gate CMOS device structures.

It is an additional object of the present invention to enhance mobility in FinFET device structures.

It is a further object of the present invention to improve methods of fabricating strained FinFET device structures.

The invention and other objects and features thereof will be more readily apparent from the following detailed description when taken in conjunction with the following drawing figures.

Brief Description of Drawings

Figures 1 and 2 schematically show perpendicular (to Fin) and parallel (to Fin) views of a FinFET according to the prior art.

Figure 3 schematically shows a perpendicular view of a FinFET semiconductor device structure according to the prior art.

Figures 4 - 17 schematically show various views of intermediate and final FinFET semiconductor device structures according to the present invention.

Best Mode for Carrying Out the Invention

The present invention is directed to a novel FinFET semiconductor device structure and a method of manufacturing such structure. A preferred final structure according to the present invention is shown in Figures 16, 17.

Referring now to the remaining figures and Figures 1 - 3 in particular, there are shown known FinFET devices (Figs. 1, 2) and device structures (Fig. 3).

To begin, standard or conventional FinFET device manufacture processing is followed through the patterning and etching of the Fins, formation of gate dielectric and conductors,

sidewall spacers (not shown), source/drain doping, and salicidation. Following salicidation, the gate sidewall spacers are removed, to facilitate the processing which will induce strain in the Fins according to the present invention.

More particularly, as described with reference to Fig. 3, an SOI wafer, for example, is provided. The SOI wafer includes a substrate **1**, disposed underneath a buried SiO_2 layer **2** as shown in Fig. 3. On top of the buried SiO_2 layer **2**, is a Silicon on Insulator (SOI) layer which is patterned into regions forming the active area of each device shown as a FIN **3** in Figs. 1, 2 and 3. The Fin may be formed by standard lithography and etching operations well known in the art. Alternatively, a known side wall image transfer method may be used to form each Fin **3**.

After the Fin has been formed, a sacrificial oxidation procedure which is well known in the art may be performed to remove any damage from the Fin etch procedure. The sacrificial oxide layer can be used as a screen to prevent channeling during well implantation, if well implantation is used to adjust the threshold voltage of the FinFET device.

The sacrificial oxide is next removed by a dry or wet etch chemistry. For example, a dilute hydrofluoric acid may be used to remove the sacrificial oxide. After the sacrificial oxide removal, a gate dielectric may be formed. The gate oxidation may be a thermal SiO_2, a nitrided SiO_2 or oxy nitride. The gate dielectric may be a high K material like TaO_5, HfO_2, or any other gate dielectric material.

The gate electrode material is next deposited on the entire wafer, after which a lithography and etching procedure may be carried out. The gate electrode is labeled electrode **4** in the diagram.

After gate formation, a reoxidation operation, which is well known in the art, may be used to improve gate dielectric characteristics. The gate re-ox may also be omitted.

At this point in the process flow, the source/drain extensions may be implanted, in another approach, an offset spacer may be used to create a distance between the gate edge and the implanted Fin region. A lithography mask may be used to block nFET regions from being implanted while allowing the pFET regions to be implanted as is common to conventional CMOS process technology. A similar operation can be used to implant the nFET regions while blocking the pFET regions.

After the source drain extension regions have been formed, an extension anneal may be used to heal the damage created by the ion implantation. In an alternate approach, the anneal may be omitted. Next, the deep source drain spacers are fabricated by depositing a SiN film in the range of 100Å to 1000Å, after which a highly directional etch is performed to remove the SiN film from the horizontal surfaces while leaving the film on the vertical portions of the gate electrode.

A block mask and ion implantation are now used to form the source and drain regions for the nFET device region **30** and pFET device region **20** as is standard in CMOS process technology. A conventional rapid thermal annealing process is next used to activate the junctions formed by the implantation. After this, a conventional salicide process using $CoSi_2$, TiSi, NiSi or any other silicide known in the art is performed.

At this point in the process flow, the inventive steps and structures (Figs. 4-17) to improve device performance for the n-FinFET and p-FinFET devices begin. First, as shown in Fig. 4 and Fig. 5, an SiO_2 liner layer (film) **5** is disposed (e.g., deposited) by, e.g., a low temperature deposition technique. The film thickness is in the range of 25-300Å and the film deposition temperature is in the range of 200-750°C. The film may be deposited by any one of a variety of different known techniques including, but not limited to, sputter deposition, Plasma Enhanced Chemical Vapor Deposition (PECVD), Rapid Thermal Chemical Vapor Deposition (RTCVD), or a standard Chemical Vapor Deposition (CVD) technique. The purpose of this SiO_2 film **5** is to act as an etch stop for a second film which is to be deposited next. Thus, the liner or etchstop layer **5** need not be SiO_2, but is any material that can provide adequate etch stop capability for the next film that is deposited directly on top of the liner

material layer **5**.

After deposition of the liner or etch stop layer **5**, a compressive film **6**, as shown in Fig. 6 and Fig. 7, is deposited over the entire wafer. In a preferred embodiment, the compressive film **6** is a SiN film deposited, e.g., by PECVD. The film **6** may also be deposited at an elevated power, in the range 400W to 1500W, to create more compression in the film. The film may be deposited using a low deposition rate and temperature range to make the film compressive. Ideally, the compression in the film is in the range of -300MPa to -3000MPa and the film thickness should be in the range of 200Å to 2000Å. Preferred deposition parameters are as follows: process temperature of 480°C, pressure of 5.75 torr, spacing between wafer and electrode of 395 mils, flow 3000 sccm of a 2% diluted SiH_4 gas, 15 sccm NH_3 gas and 1060 sccm N gas using an RF power of 900 Watts. This process yields a deposition rate of approximately 15.95Å/s and a film stress of about (±10%) -1400 MPa.

After the compressive film **6** has been applied to the wafer, a block mask **7**, as shown in Fig. 8 and Fig. 9, is used to mask to pFET regions of the wafer. This block mask may be formed by conventional lithographic techniques known in the art. The mask is formed by a conventional lithography procedure in which a photosensitive material is coated over the wafer surface and exposed through a mask. The photosensitive material is then developed, leaving resist images or features blocking the pFET areas on the wafer.

After formation of the block mask **7**, the compressive film **6** is removed by a known wet etching or dry etching technique that is capable of removing the compressive film selectively with respect to the block mask material. A plasma consisting of CH_2F_2 is an example of a dry etch chemistry that may be used for this purpose if the compressive film is SiN. After the compressive film has been removed from the nFET regions on the wafer, an intermediate structure appears as shown in Fig. 10 and Fig. 11.

At this point in the inventive process flow, the block mask **7** is removed from the wafer using a solvent or O_2 plasma process known in the art to remove resist or organic materials. Next, a second liner or etchstop material **8** is deposited on the entire wafer as shown in Figs.

12 and 13. The second liner layer **8** has at least similar properties as the first liner previously described. That is, the liner is to be used as an etch stop for a subsequent film etching process.

Next, a tensile film **9** is deposited over the entire wafer as shown in Fig. 14 and Fig. 15. The tensile film is, e.g., SiN and is deposited by, e.g., CVD, PECVD, RTCVD or any other deposition technique capable of depositing a highly tensile film. The film thickness should be in the range of 200Å to 2000Å, and the stress should be in the range +200MPa to +2000MPa or more tensile. Preferred deposition parameters are:
process temperature of 480°C, pressure of 6.25 torr, spacing between wafer and electrode of 490 mils, flow 3000 sccm of a 2% dilute SiH_4 gas, 15 sccm NH_3 gas and 1060 sccm N gas using an RF power of 340 Watts. This process yields a deposition rate of approximately 23Å/s and a film stress of about
500 MPa.

At this point in the inventive process flow, a block mask **10** is patterned over the nFET regions of the wafer as shown in Fig. 16. The properties of this block mask are similar to the properties of the block mask previously described to block the pFET regions. After the block mask has been defined, a known wet or dry etching procedure is carried out to remove the tensile film **9** from the pFET regions. The etch should be selective to the liner etch stop material **8**. In this way, the etch used to remove the tensile film from the nFET regions does not remove the compressive film which is present on the pFET regions. The block mask is next removed using a similar methodology used to remove the first block mask, to result in the final device structure **200, 300** shown in Fig. 17.

At this point in the inventive process flow, a thin film (not shown) in the range of 50Å to 500Å, with a low stress in the range of -100 MPa compressive to +100 MPa tensile may be applied to the wafer to serve as a barrier layer. The purpose of this thin film is to fill in any regions not covered by the compressive or tensile films. This optional film may be used to improve the suppression of contamination from penetrating into the Si and also help to improve the etch stop characteristics for the source-drain contact etch.

After the operations described above are carried out, the CMOS process may be continued using standard process methodologies (not shown) well known in the art. More specifically, the processing that follows includes: deposition and planarization of a glass layer (i.e., BPSG, TEOS); etching of source/drain contacts, deposition of contact metallurgy and planarization; additional levels of insulating layers, vias, and wiring are then formed to complete the chip.

The presence of the stressed films on the longitudinal sidewalls of the Fins, overlying the gate conductors, results in a stress in the channel which is of the same type as the stress in the film (i.e., compressive/compressive, tensile/tensile). The stress in the source/drain regions on the longitudinal sidewalls of the Fins is of opposite type (i.e., compressive/tensile, tensile/compressive). To access the source/drain diffusions, the films on the top surface of each Fin may be removed without negating the effects of the film on the longitudinal sidewalls.

While there has been shown and described what is at present considered a preferred embodiment of the present invention, it will be apparent to those skilled in the art that various changes and modifications may be made therein without departing from the spirit and scope of the present invention.

Industrial Applicability

The present invention is applicable to microelectronic semiconductor devices.

Claims

1. A semiconductor device structure, comprising:

a PMOS device **200** and an NMOS device **300** disposed on a substrate **1,2**,

the PMOS device **200** including a compressive layer **6** stressing an active region **3** of the PMOS device,

the NMOS device **300** including a tensile layer **9** stressing an active region **3** of the NMOS device, wherein

the compressive layer includes a first dielectric material **6**, the tensile layer includes a second dielectric material **9**, and the PMOS and NMOS devices are FinFET devices **200,300**.

2. The semiconductor device structure as claimed in claim 1, wherein the first dielectric material comprises SiN.

3. The semiconductor device structure as claimed in claim 1, wherein the second dielectric material comprises SiN.

4. The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform compressive stress in a range of -300 MPa to -3000 MPa.

5. The semiconductor device structure as claimed in claim 1, wherein the first dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

6. The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform tensile stress in a range of +200 MPa to +2000 MPa.

7. The semiconductor device structure as claimed in claim 1, wherein the second dielectric material has a substantially uniform thickness in a range of 200Å to 2000Å.

8. The semiconductor device structure as claimed in claim 1, wherein the first dielectric material and the second dielectric material are SiN.

9. A method for manufacturing a semiconductor device structure, comprising:

providing a p-FinFET device region **200** and an n-FinFET device region 300 on a same substrate **1, 2**;

disposing a first liner **5** on the p-FinFET device region and the n-FinFET device region;

disposing a compressive film **6** on the first liner;

disposing a first mask **7** on the p-FinFET device region;

removing the compressive film from the n-FinFET device region;

removing the first mask **7**;

disposing a second liner **8** on the p-FinFET device region and the n-FinFET device region;

disposing a tensile film **9** on the second liner;

disposing a second mask **10** on the n-FinFET device region;

removing the tensile film from the p-FinFET device region; and

then removing the second mask.

10. The method as claimed in claim 9,

wherein said step of disposing a compressive film includes depositing a compressive film having a film stress of about -1400 MPa.

11. The method as claimed in claim 9,

wherein said step of disposing a tensile film includes depositing a tensile film having a film stress of about +500 MPa.

12. The method as claimed in claim 9, wherein the compressive film is SiN.

13. The method as claimed in claim 9, wherein the tensile film is SiN.

14. The method as claimed in claim 9,

wherein the compressive film is disposed having a substantially uniform thickness in a range of 200Å to 2000Å.

15. The method as claimed in claim 9,

wherein the tensile film is disposed having a substantially uniform thickness in a range of 200Å to 2000Å.

16. The method as claimed in claim 9,

wherein said step of disposing a compressive film includes depositing a compressive film having a film stress of greater than about -1400 MPa.

17. The method as claimed in claim 9,

wherein said step of disposing a tensile film includes depositing a tensile film having a film stress of greater than about +500 MPa.

Perp. to Fin view

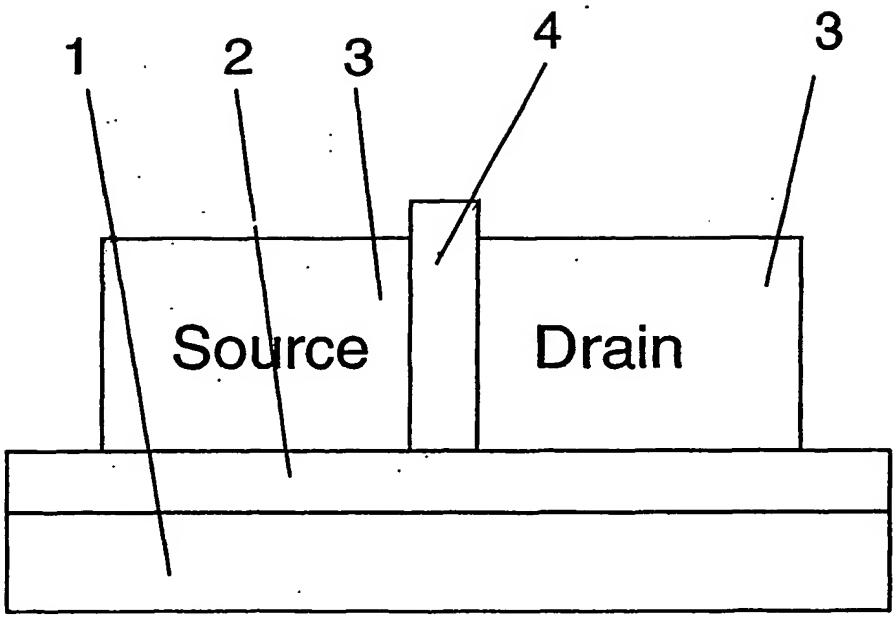


Fig 1
Prior Art

Parallel to Fin view

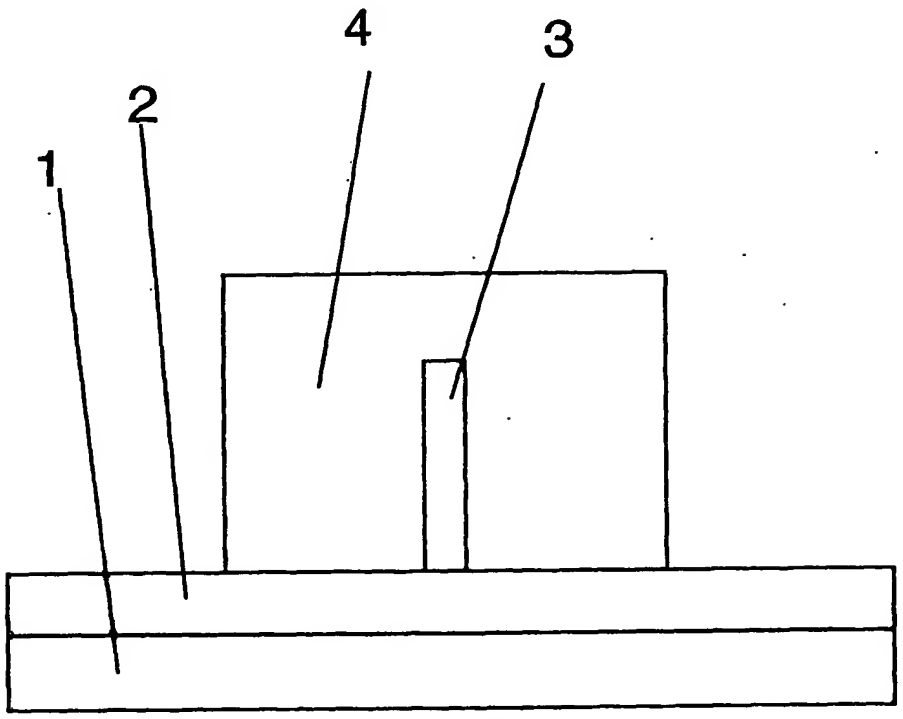


Fig 2
Prior Art

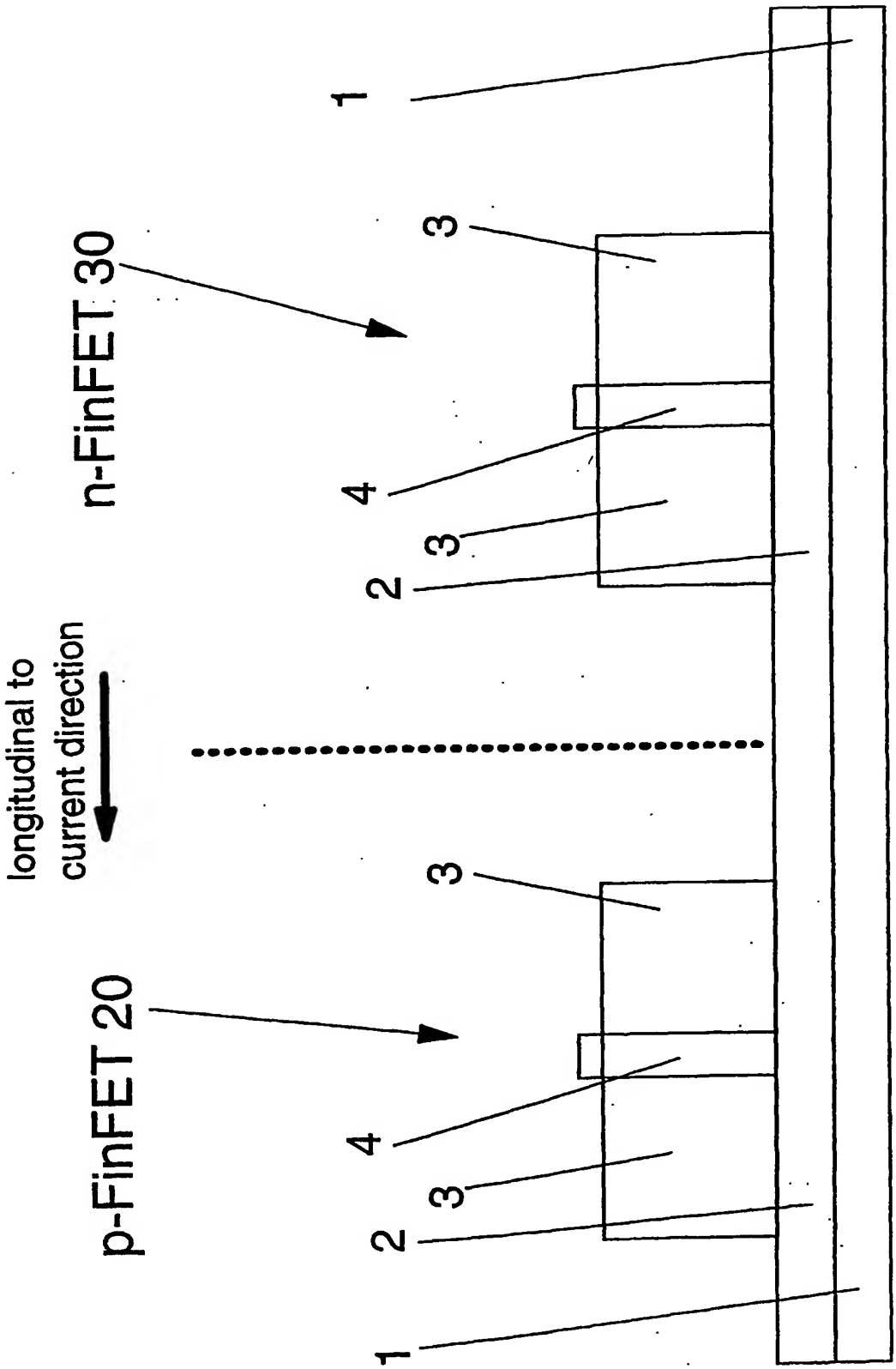


Fig 3
Prior Art

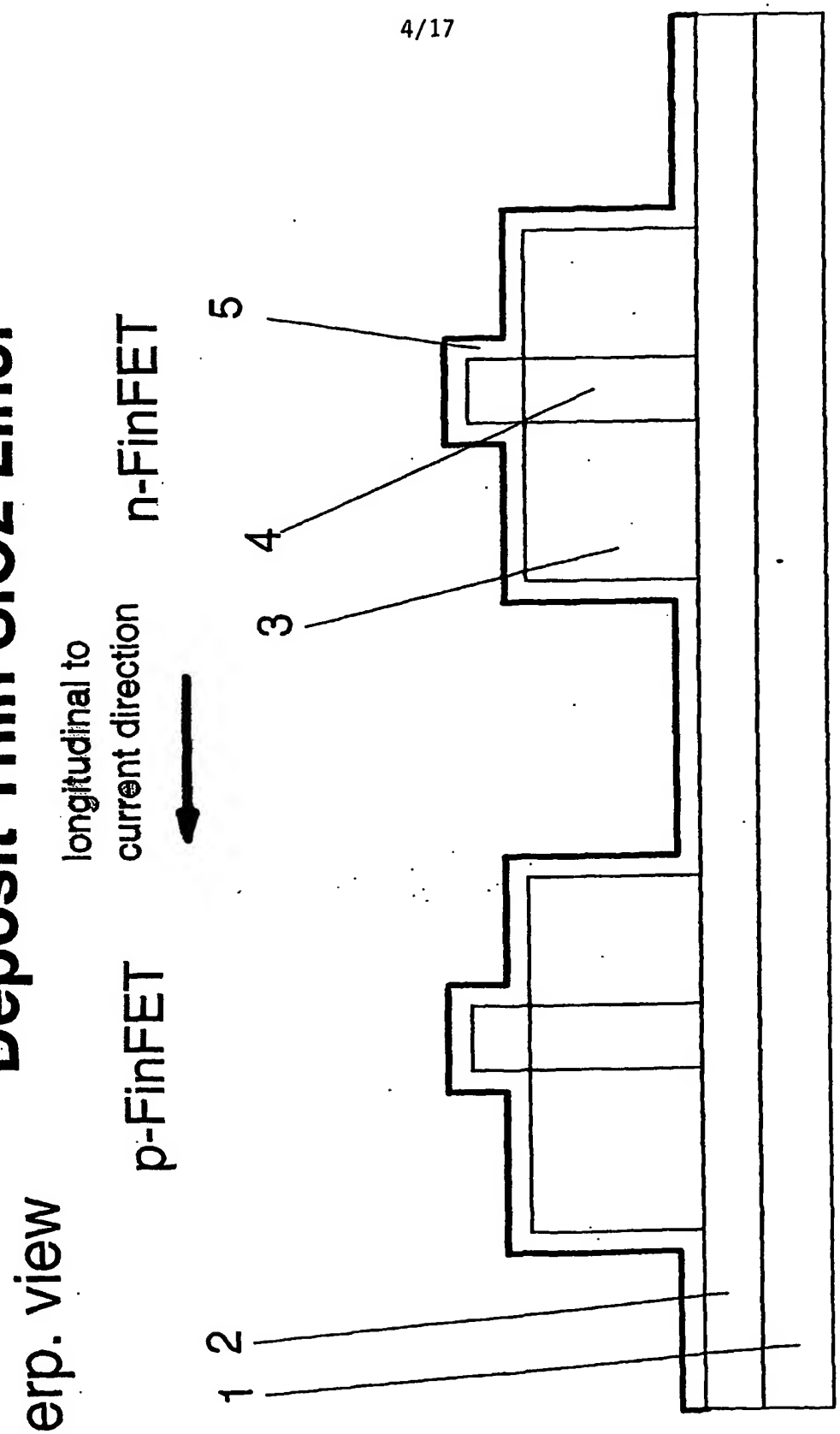

Deposit Thin SiO2 Liner
Perp. view
p-FinFET
longitudinal to current direction
n-FinFET
1
2
3
4
5

Fig 4

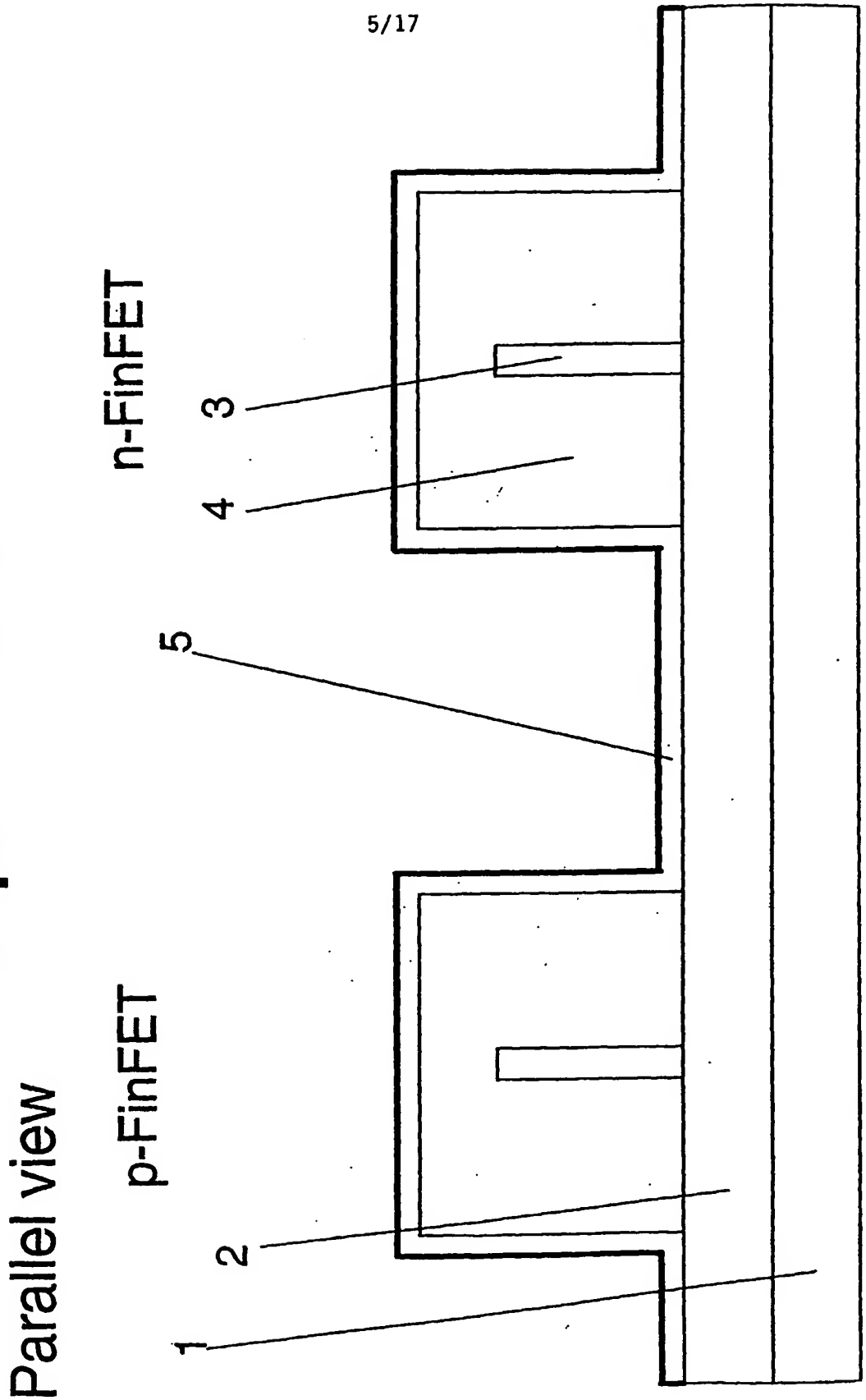

Deposit Thin SiO2 Liner
Parallel view
p-FinFET
n-FinFET
1
2
3
4
5

Fig 5

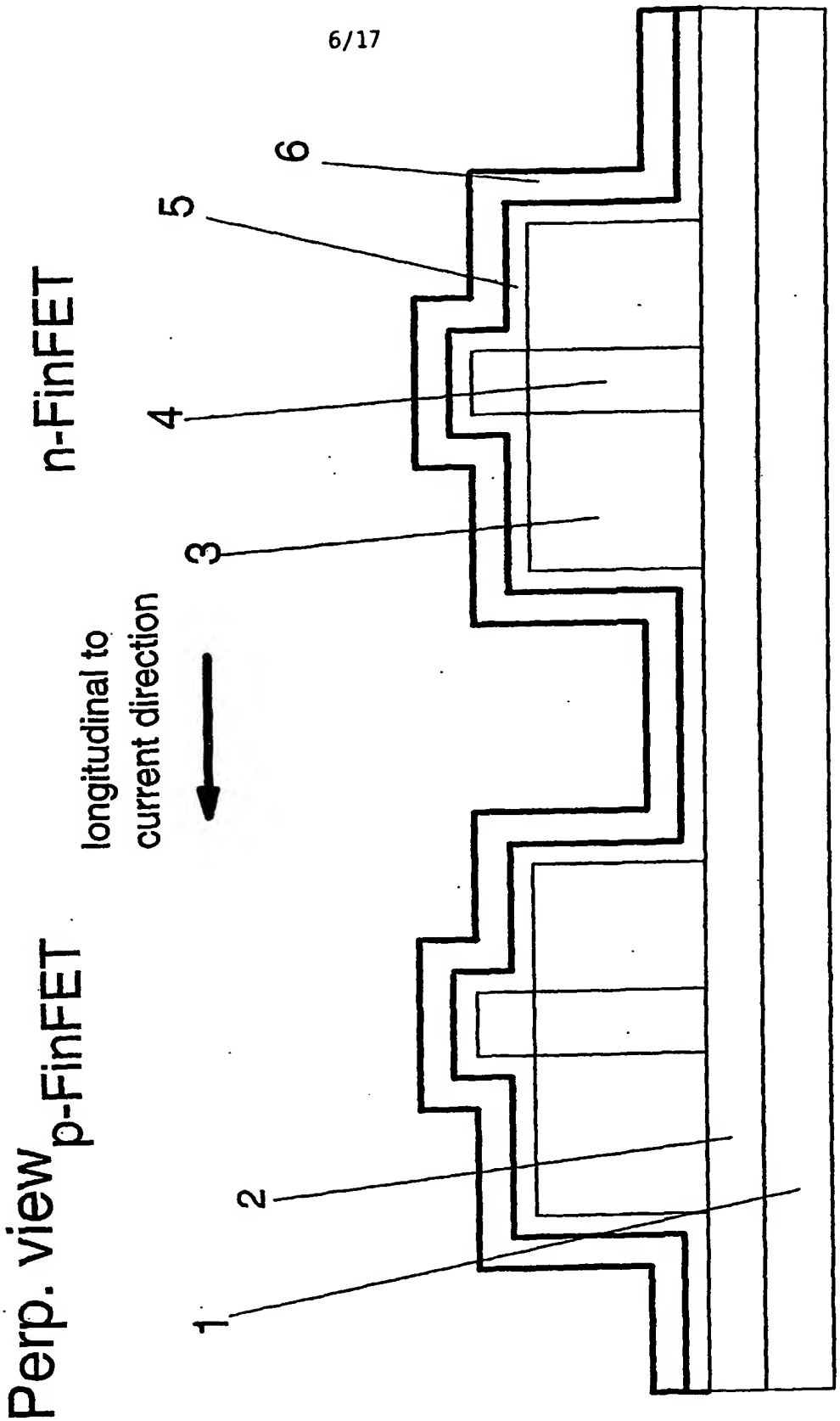

Deposit Compressive Film
Perp. view
p-FinFET
n-FinFET
longitudinal to
current direction
1
2
3
4
5
6

Fig 6

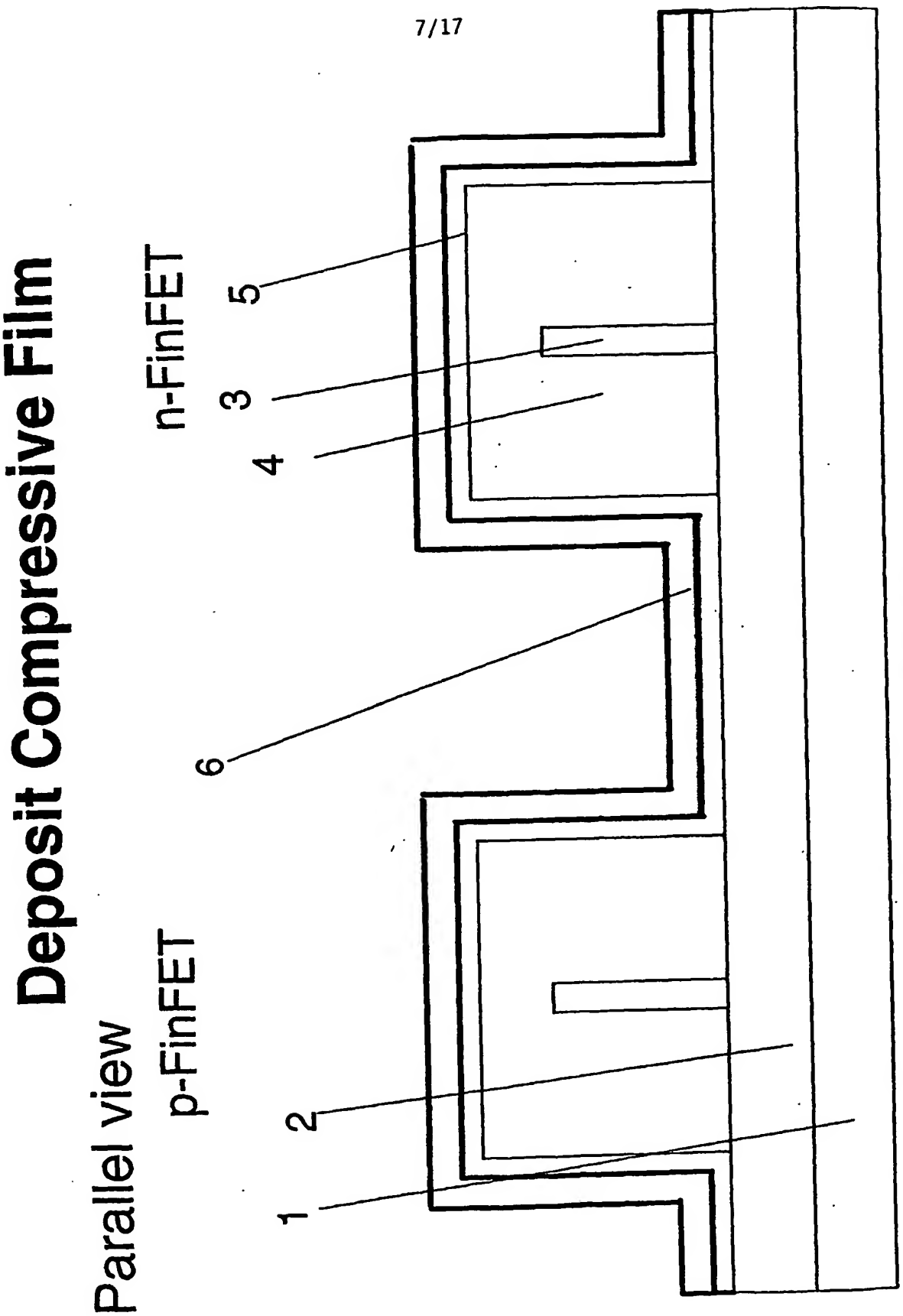

Deposit Compressive Film
Parallel view
p-FinFET
n-FinFET
1
2
3
4
5
6

Fig 7

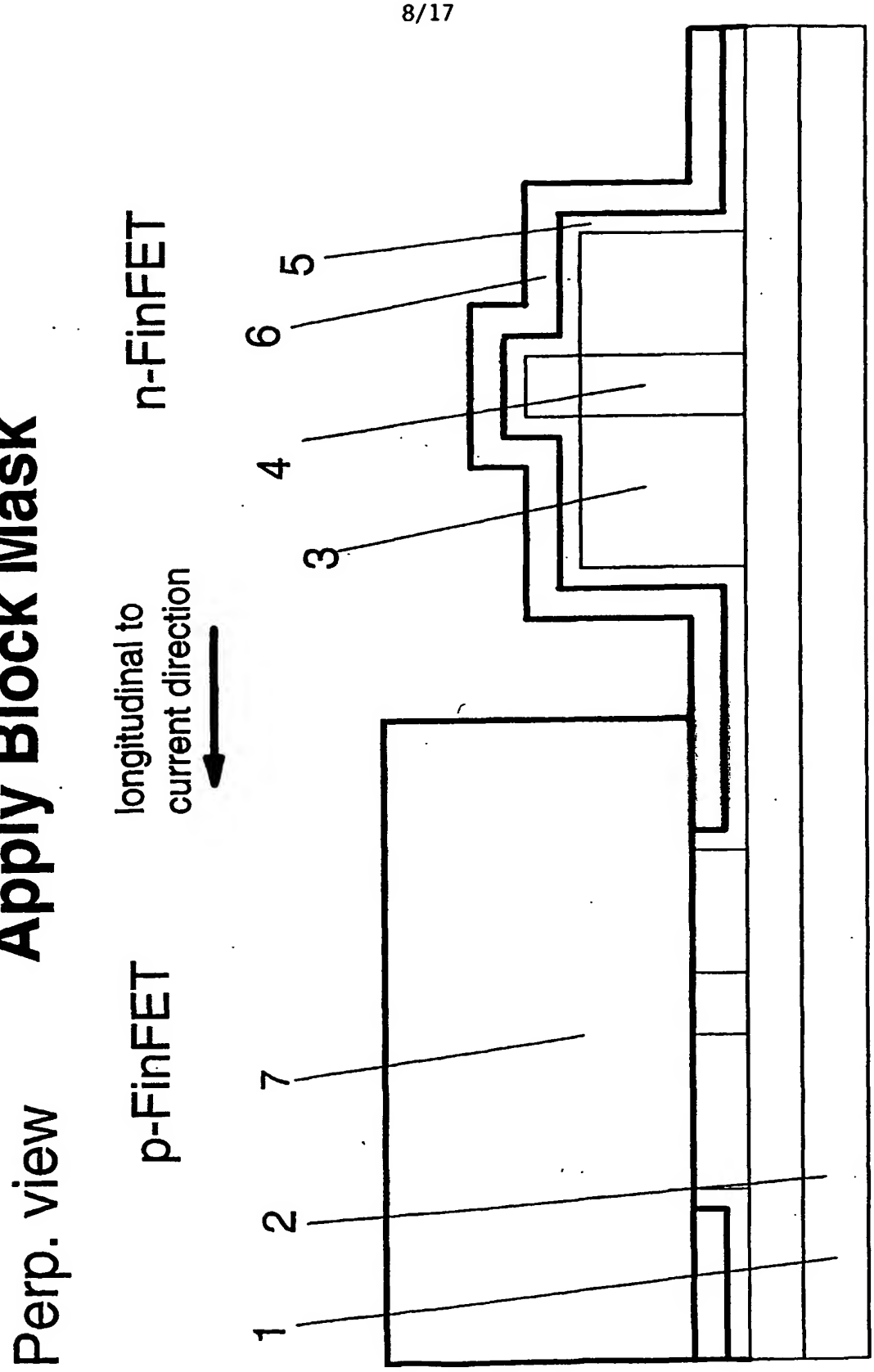

Apply Block Mask
Perp. view
p-FinFET
n-FinFET
longitudinal to current direction
1
2
3
4
5
6
7

Fig 8

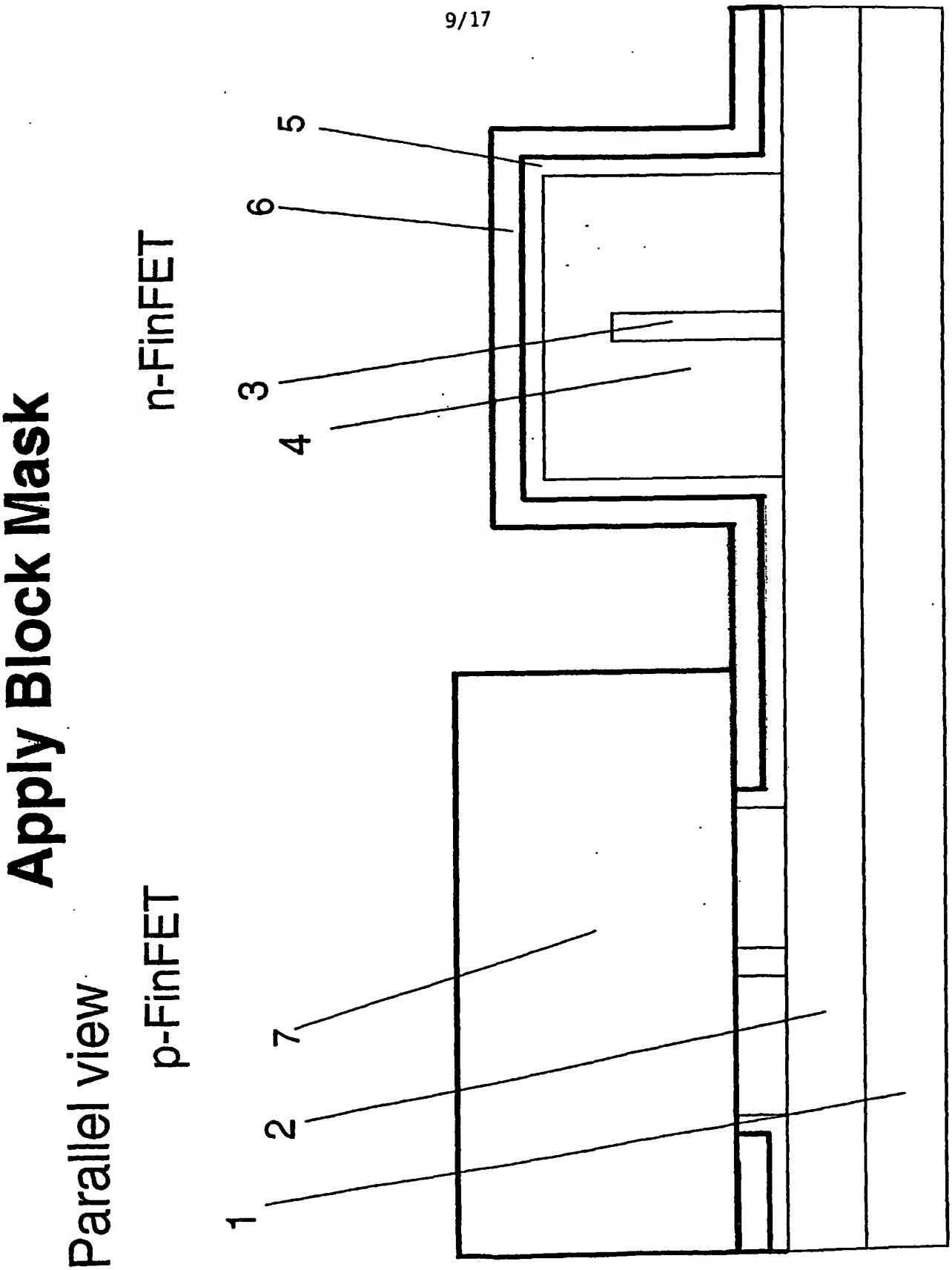


Fig 9

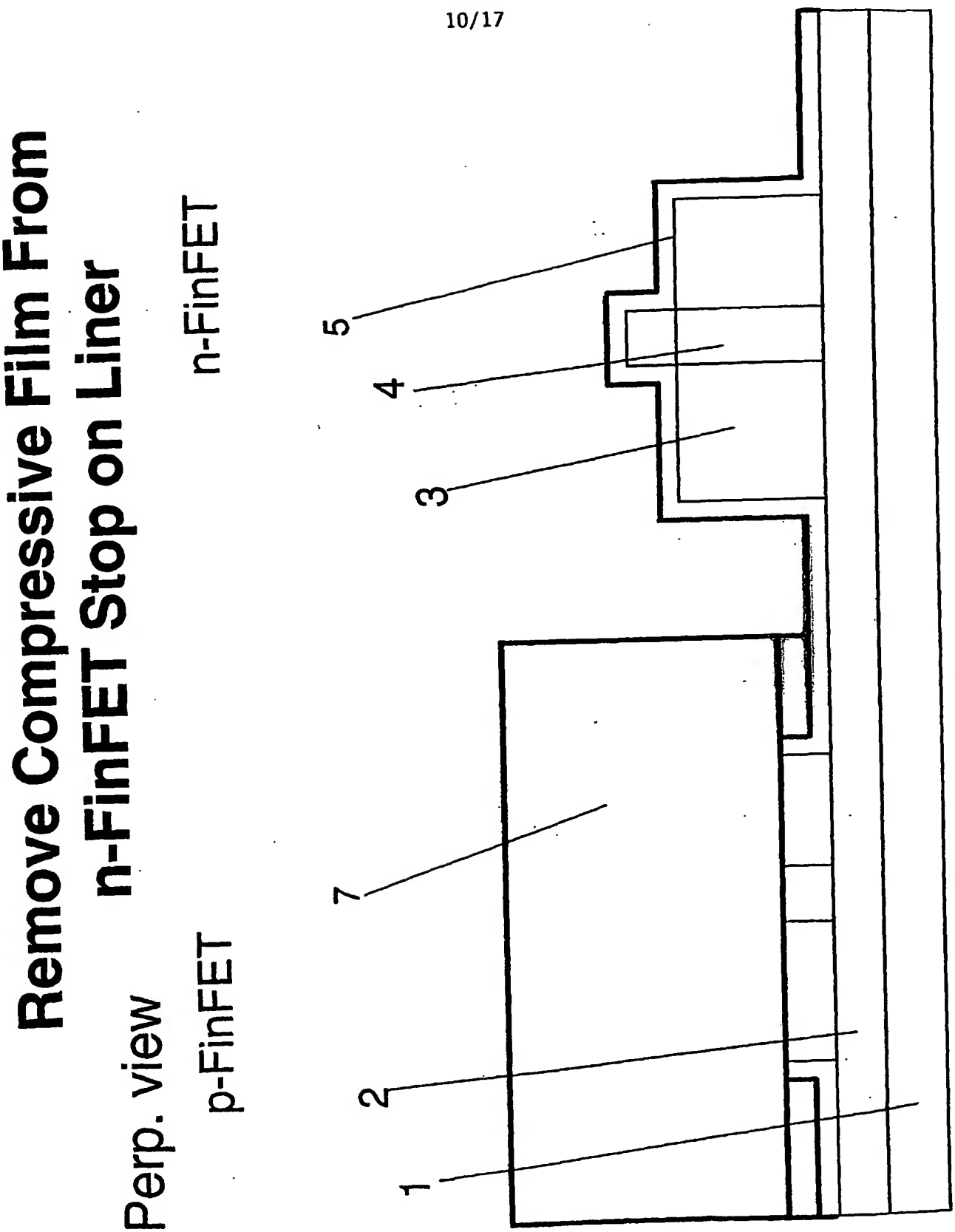

Remove Compressive Film From
n-FinFET Stop on Liner
Perp. view
p-FinFET
n-FinFET
1
2
3
4
5
7

Fig 10

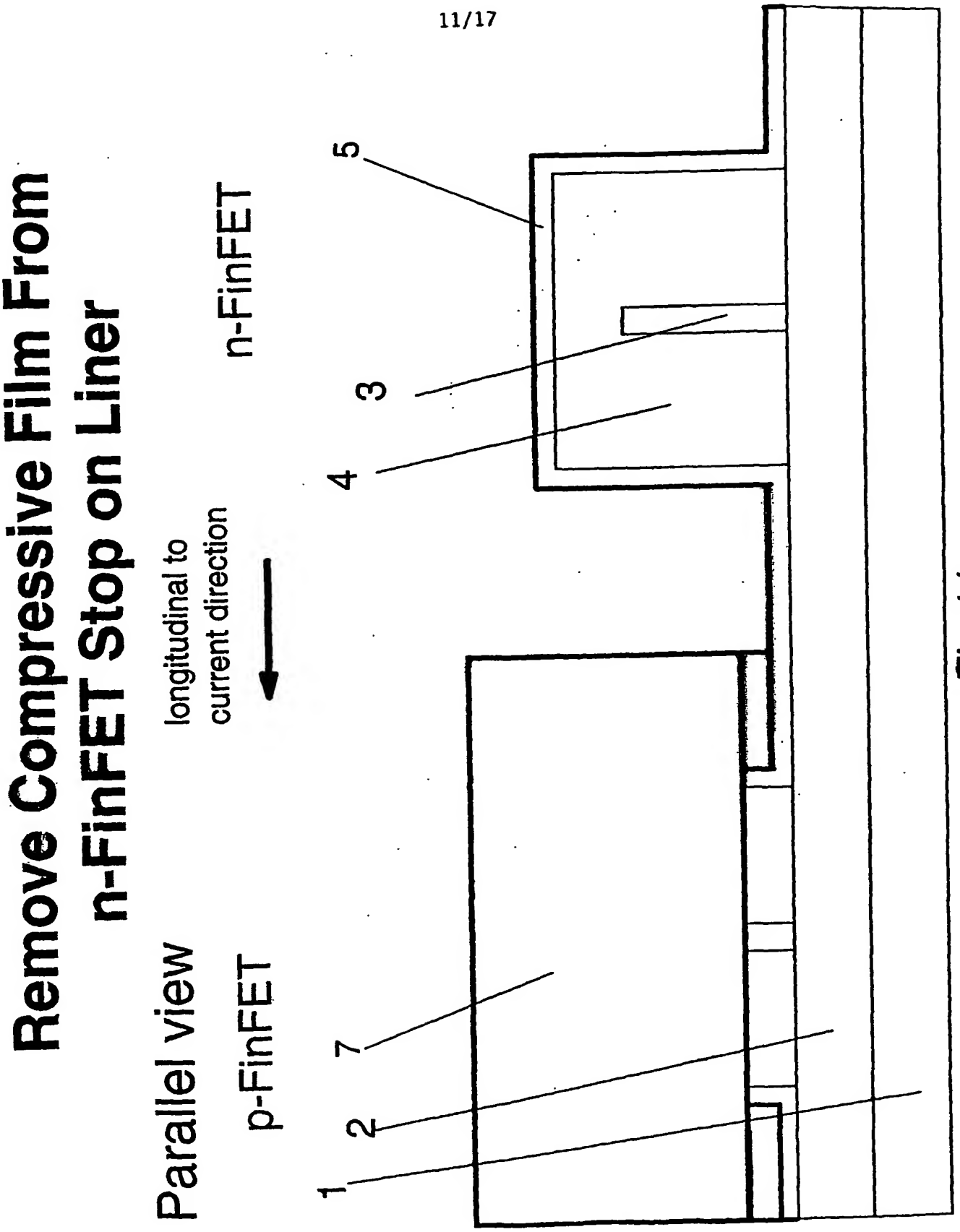

Remove Compressive Film From
n-FinFET Stop on Liner
Parallel view
p-FinFET
n-FinFET
longitudinal to
current direction
1
2
3
4
5
7

Fig 11

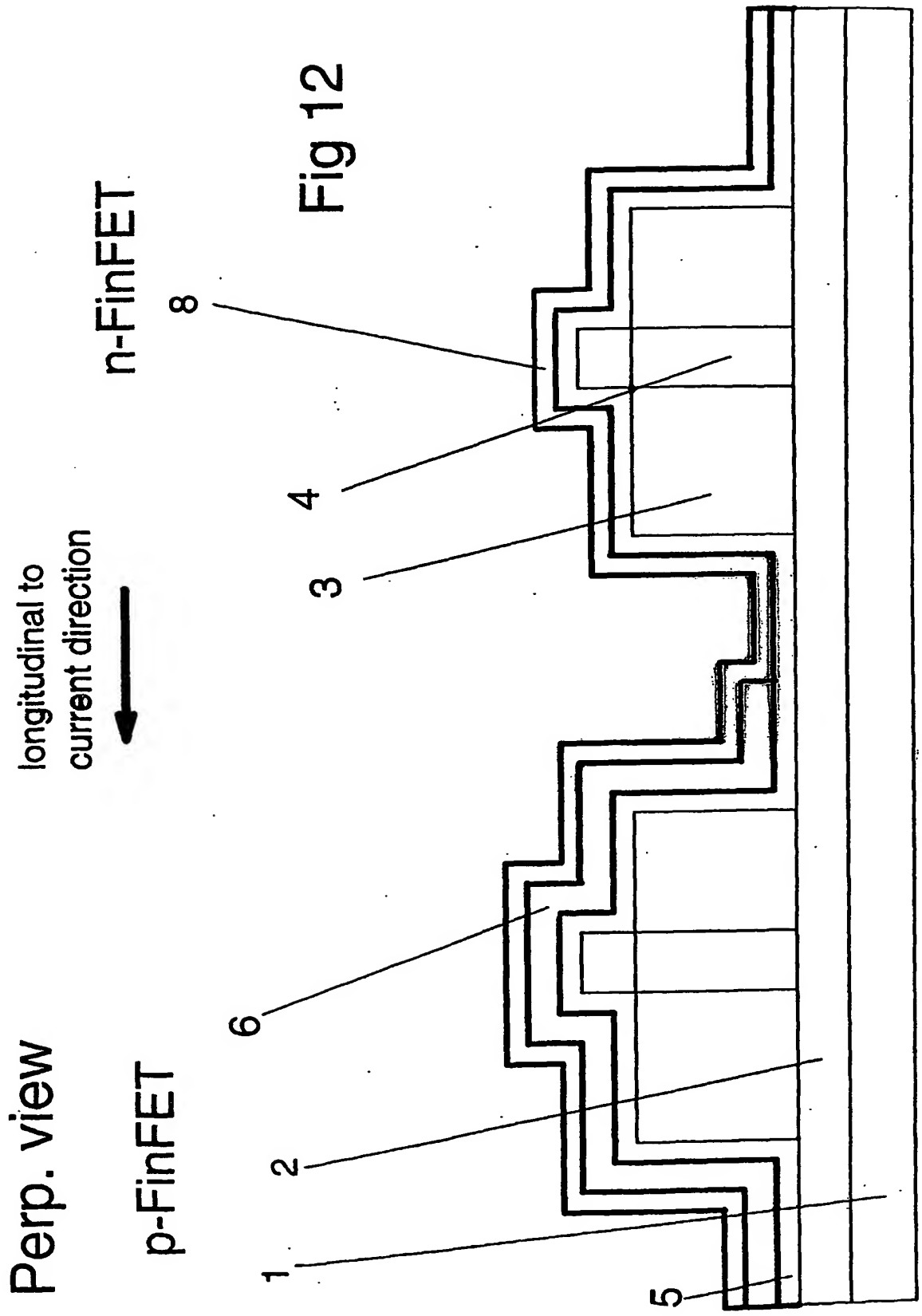

Remove Block Mask, Optional Liner 1 Removal, Deposit 2nd thin liner
Perp. view
p-FinFET
n-FinFET
longitudinal to current direction
1
2
3
4
5
6
8

Fig 12

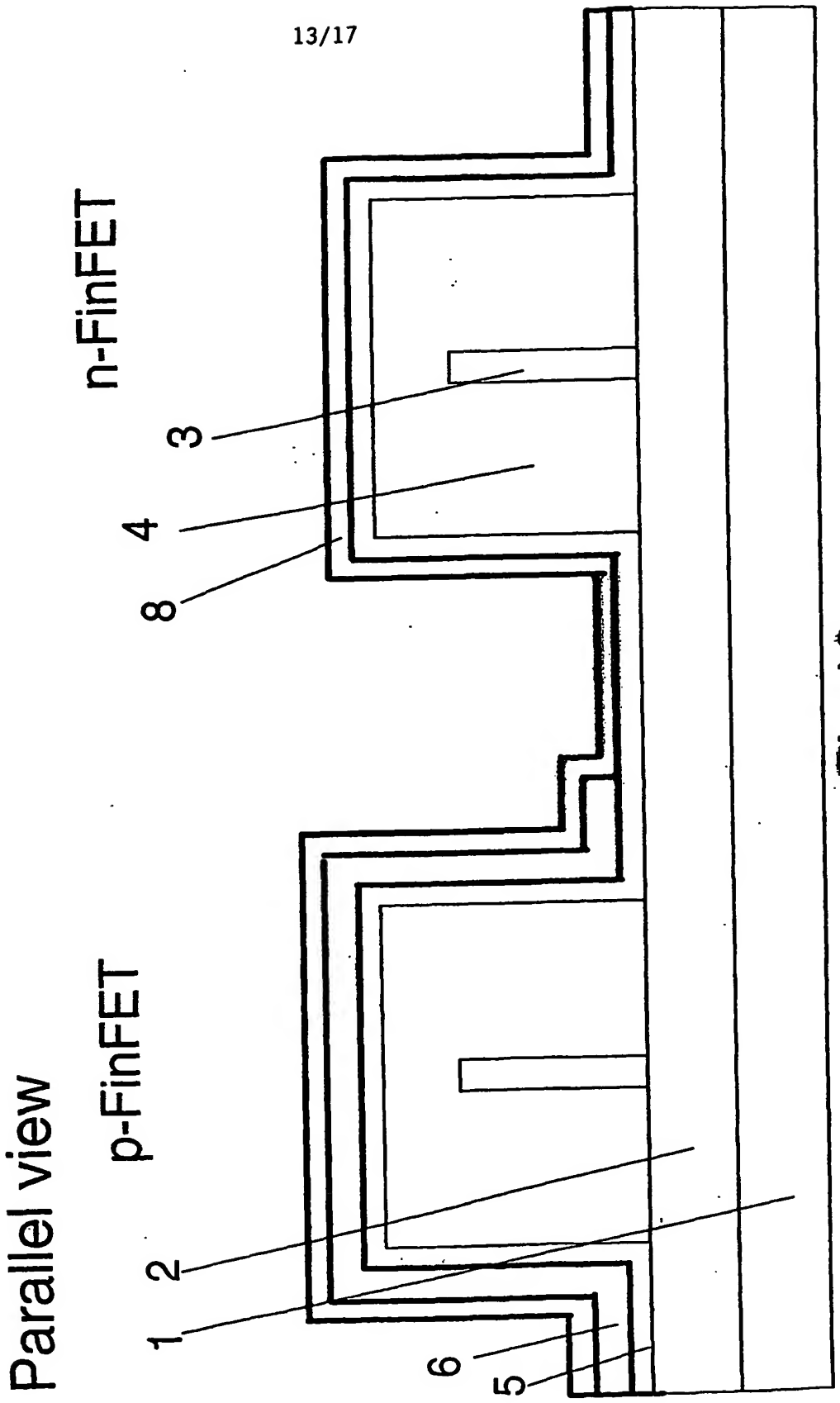

Remove Block Mask, Optional Liner 1 Removal, Deposit 2nd Thin Liner
Parallel view
p-FinFET
n-FinFET
1
2
3
4
5
6
8

Fig 13

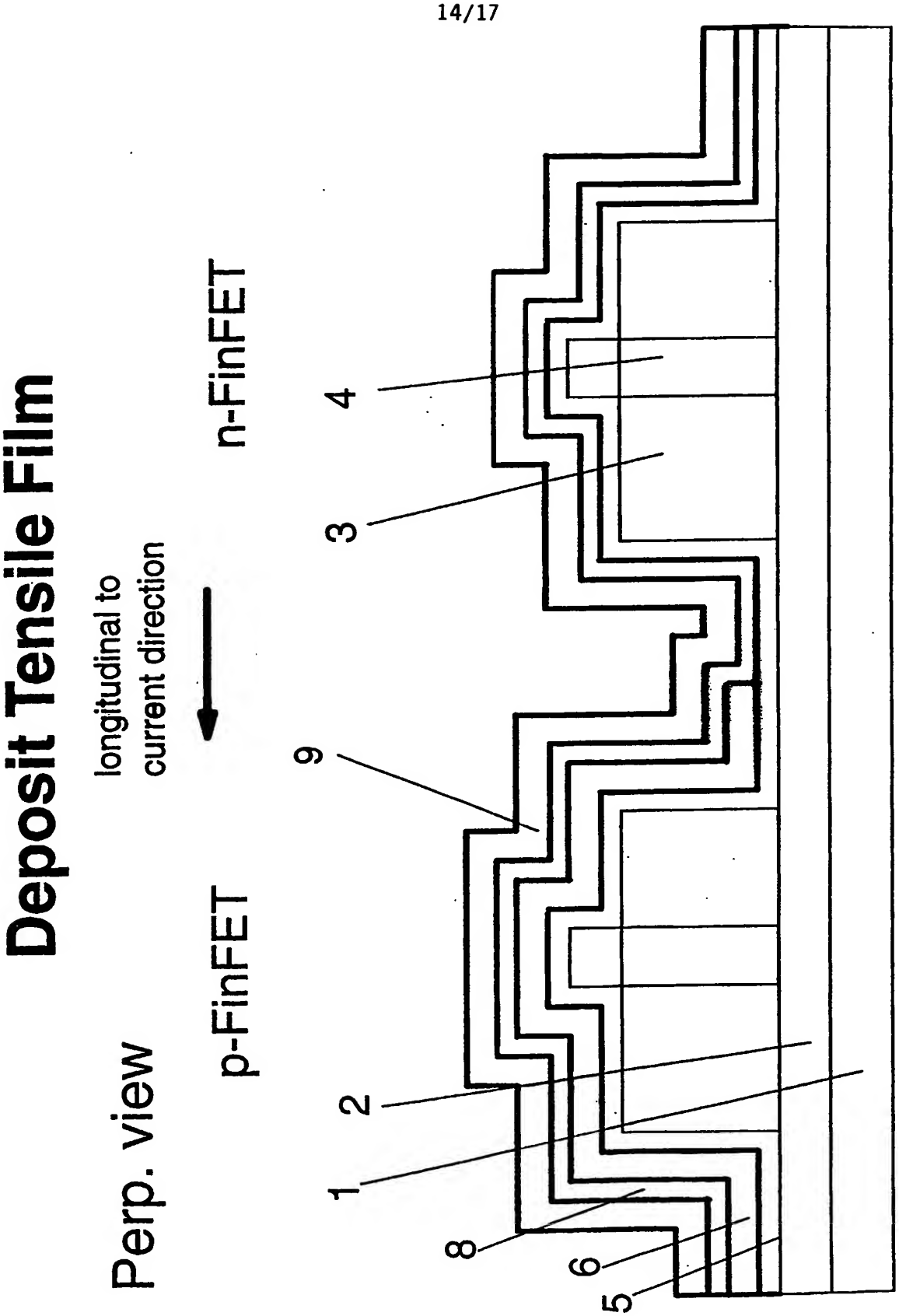

Deposit Tensile Film
Perp. view
longitudinal to current direction
p-FinFET
n-FinFET
1
2
3
4
5
6
8
9

Fig 14

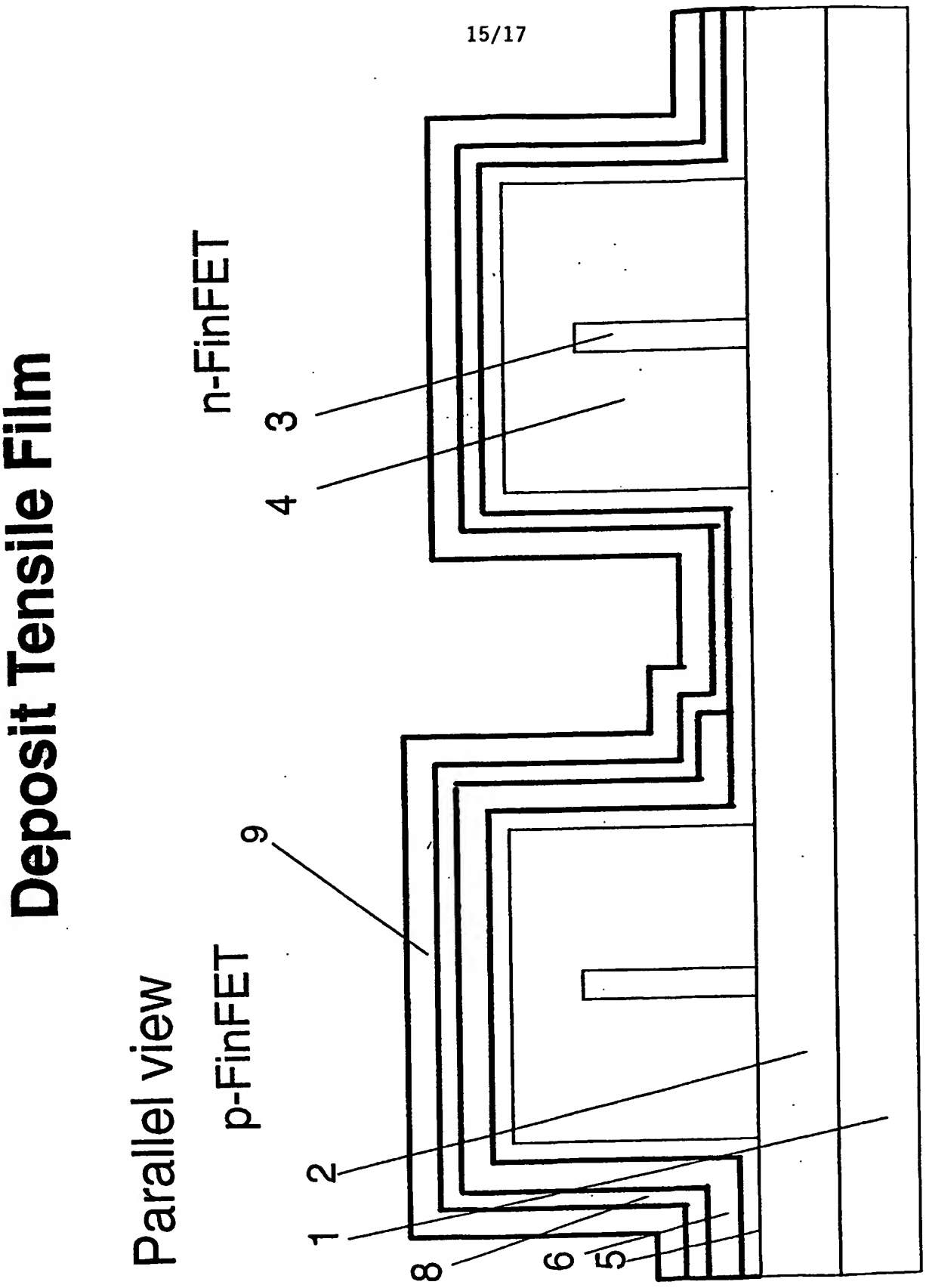

Deposit Tensile Film
Parallel view
p-FinFET
n-FinFET
1
2
3
4
5
6
8
9

Fig 15

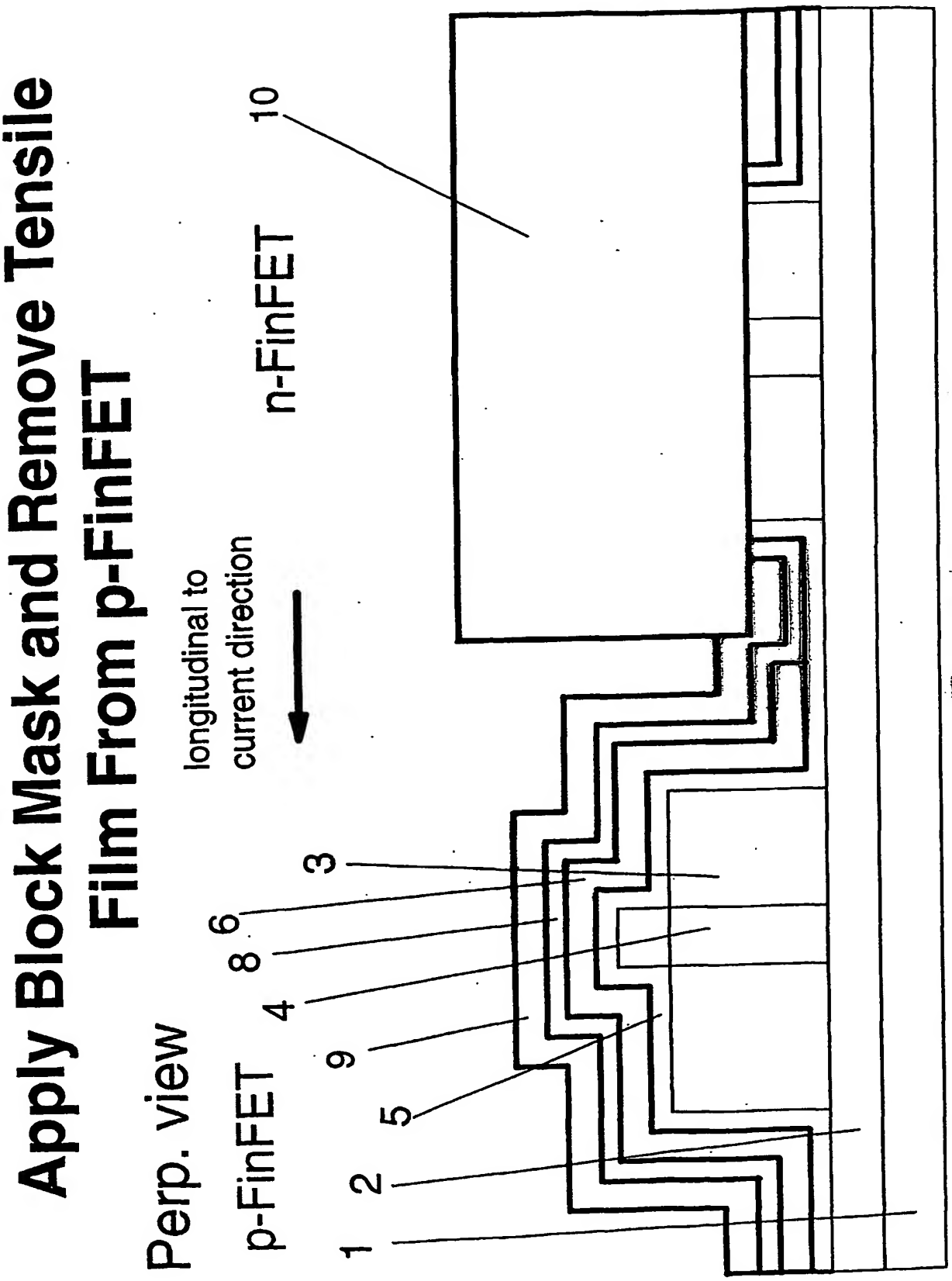

Apply Block Mask and Remove Tensile Film From p-FinFET
Perp. view
p-FinFET
n-FinFET
longitudinal to current direction
10
1
2
5
9
4
8
6
3

Fig 16

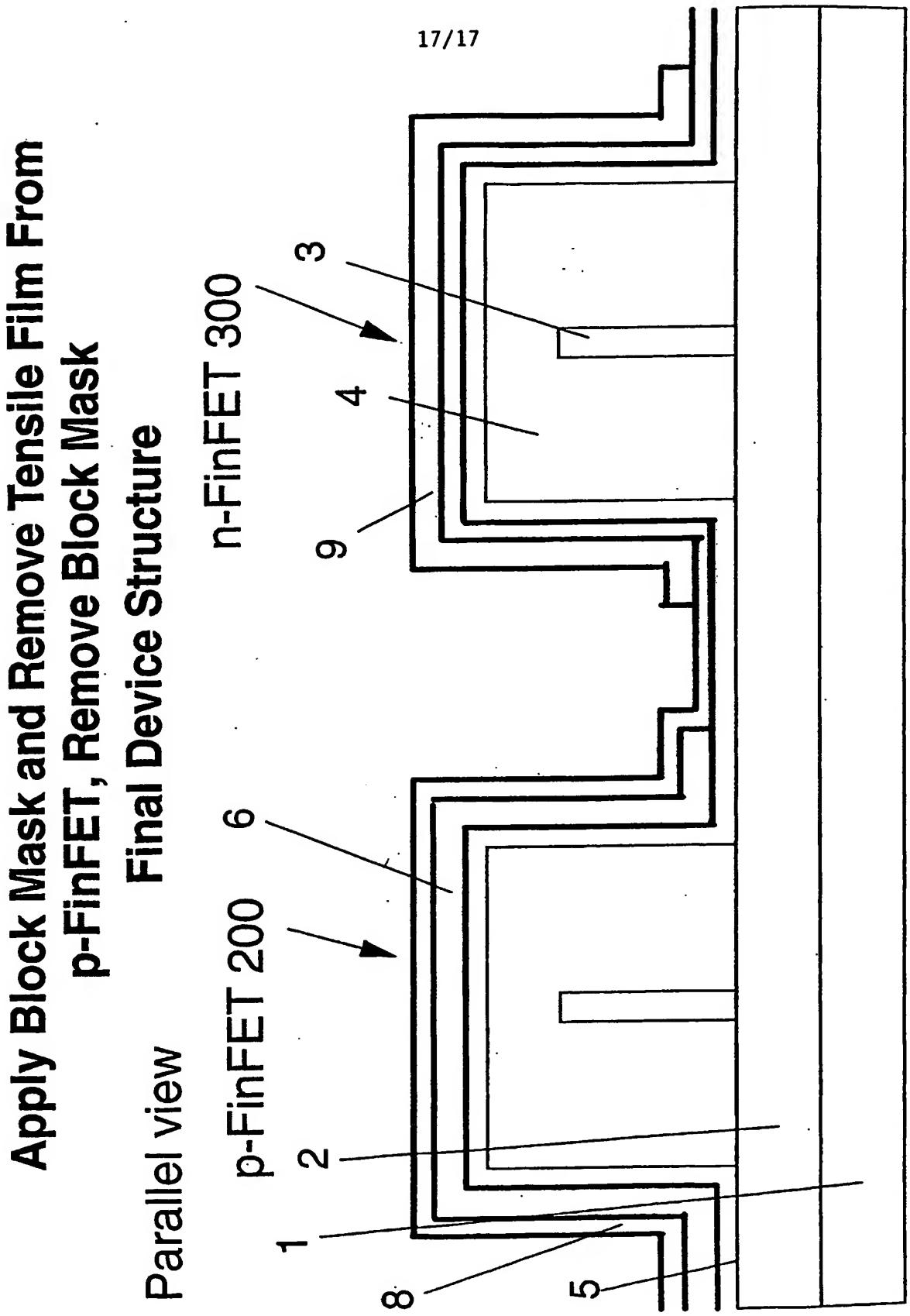

Apply Block Mask and Remove Tensile Film From p-FinFET, Remove Block Mask
Final Device Structure
Parallel view
p-FinFET 200
n-FinFET 300
1
2
3
4
5
6
8
9

Fig 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/37931

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/00
US CL : 438/164

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/164

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,342,410 B1 (YU et al.) 29 January 2002 (29.01.2002).	1-17
A	US 6,413,802 B1 (HU et al.) 02 July 2002 (02.06.2002).	1-17
A	US 6,433,609 B1 (VOLDMAN) 13 August 2002 (13.08.2002).	1-17
A	US 6,458,662 B1 (YU) 01 October 2002 (01.10.2002).	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 December 2002 (30.12.2002)	07 MAR 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer John Nieblin[illegible] Telephone No. (703) 308-1782

Deborah P. Vega
Paralegal Specialist
Technology Center 2800
(703) 308-3078

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

PCT/US02/37931

Continuation of B. FIELDS SEARCHED Item 3:
EAST
serach terms: Finfet, compression, tension